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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,603	02/19/2004	Osamu Aizawa	1614.1384	3177

21171 7590 11/30/2006

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,603	AIZAWA, OSAMU	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) *5 and 6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 7* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Potter et al. (U.S. Patent 6,533,587) in view of Reimer (U.S. Patent 4,498,717).

As to claims 1, 7, Potter et al. discloses a printed board unit of an electronic apparatus as shown in figure 1 comprising:

a mother board (20, column 3, lines 18-19); and

first and second board units (12, 14) that are vertically mounted onto the mother board (20) and face each other,

the first board unit including a vertically standing daughter board (12), and an electronic parts mounting board (14) that horizontally protrudes from the daughter board,

the second board unit including vertically standing daughter board (12), and an electronic parts mounting board (14) that horizontally protrudes from the daughter board,

the electronic parts mounting boards (14) of the first and second board units facing each other.

Potter et al. does not disclose the mounting board of each of the board units that being positioned in different height, and overlapping with each other when seen from the tops of the daughter boards.

Reimer teaches an arrangement comprising first and second raiser boards (14, 15) connected to a board (51), each having an electronic board (1) positioned in different height, facing and overlapping with each other.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have teaching of Reimer applied on the PCB unit of Potter in order to provide an easy installation, save space, and easy to trouble shoot if one of the cards to be fails on test.

As to claim 2, Potter et al. discloses a printed board unit as shown in figure 1 comprising:

a mother board (20); and

first board unit and second board units (12, 14) that are vertically mounted onto the mother board (20) and face each other,

the first board unit including a vertically standing daughter board (12) having a connector (13), and an electronic parts mounting board (14) connected to the daughter board (12) by the connector (13) and horizontally protrudes from the daughter board (12),

the second board unit including vertically standing daughter board (12) having a connector (13), and an electronic parts mounting board (14) connected the daughter

board (12) by the connector (13) and horizontally protrudes from the daughter board (12),

Potter does not discloses the connectors (13) of the first and second board units being formed on lower and upper regions of each of the daughter boards (12), and overlapping with each other when seen from the tops of the daughter boards.

Reimer teaches an arrangement comprising first and second raiser boards (14, 15) connected to a board (51), each having an electronic parts board (1) connected to a connector that being formed in different position, the board (1) facing and overlapping with each other.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have teaching of Reimer applied on the PCB unit of Potter in order to provide an easy installation, save space, and easy to trouble shoot if one of the cards to be fails on test.

As to claim 4, Potter et al. discloses a semiconductor part (components formed on the motherboard 20) mounted between the daughter boards of the first and second board units on mother board (20); and the semiconductor part is accommodated a space that is formed below the electronic parts mounting board of the first board unit, see figure 1.

Allowable Subject Matter

3. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments with respect to claims 1-4, and 7 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Enad Elvin can be reached on 571-272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan Dinh
November 24, 2006.